



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,676	07/02/2003	Thomas C. Anthony	10014296-1	3426

7590 04/25/2005

HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, CO 80527-2400

EXAMINER

TRAN, LONG K

ART UNIT	PAPER NUMBER
----------	--------------

2818

DATE MAILED: 04/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

11A

<b>Office Action Summary</b>	Application No. 10/612,676	Applicant(s) ANTHONY ET AL.	
	Examiner Long K. Tran	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 and 18-32 is/are pending in the application.
- 4a) Of the above claim(s) 18-28 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 29-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. ____   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____  | 6) <input type="checkbox"/> Other: ____                                     |

## DETAILED ACTION

### *Response to Amendment*

1. This office action is in response to Amendment filed on February 25, 2005.
2. Claims **13 – 17** and **33** have been cancelled.
3. Claims **1 – 12** and **18 – 32** are presented for examination.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **1 – 3**, **8** and **9** are rejected under 35 U.S.C. 102(e) as being anticipated by Childress et al. (US Patent Application Publication No. 2003/0231437).
6. Regarding claim **1**, Childress et al. disclose a memory wafer ([0018]) comprising:  
a first surface of 9, 109 (figs. 1 & 2) having memory chips disposed thereon, the memory chip defining an exterior face 150 (fig. 2) of the memory wafer (note: the MTJ is use in nonvolatile memory elements or cells for MRAM ([0002]); substrate 9 (fig. 1) would be a silicon (memory) wafer if the device is a memory cell ([0018]). Therefore, it is fair to say that the silicon wafer 9 having memory chips for MRAM).

A second surface of 9, 109 (figs. 1 & 2) opposite the exterior face; and

A top magnetically permeable shield layer (made of permalloy (NiFe) as the claimed permeable shield layer) on top of surface 150 (not shown) ([0021]).

Regarding claim 2, Childress et al. disclose the memory chips are separable from the memory wafer (fig. 1).

Regarding claim 3, Childress et al. disclose the memory chips are MRAM ([0002]).

Regarding claims 8 and 9, Childress et al. disclose the magnetically permeable layer is a permalloy (NiFe) and is a soft magnetic material.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 4, 5, 6, 7, 10, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Childress et al. (US Patent Application Publication No. 2003/0231437) in view of Rizzo et al. (US Patent Application Publication No. 2004/0000415).

9. Regarding claim 4, Childress et al. disclose the claimed invention of claim 1 except for the memory chips include multiple memory arrays having multiple memory cells.

It is conventional and also shown by Rizzo et al. that MRAM including an array of magnetic memories ([0025]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to understand that Childress's device would comprise multiple memory arrays having multiple memory cells since it was known in the art that MRAM including cells in array.

Regarding claim **5**, Childress et al. disclose the memory cells are magnetic random access cells ([0002], [0018]).

Regarding claims **6** and **7**, Rizzo et al. disclose integrated circuit 15 (fig. 1; ([0025]) including contact pads capable of transmitting signals to and from circuit 15 ([0025]).

Regarding claim **10**, Rizzo et al. disclose the magnetically permeable shield layer has a permeability of 1,000 – 10,000 ([0053]).

Regarding claim **11**, Rizzo et al. disclose the magnetically permeable shield layer has a coercivity of less than 10 Oersteds ([0043]).

Regarding claim **12**, Rizzo et al. disclose the magnetically permeable shield layer is isotropic ([0053]).

10. Claims **29** and **30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Childress et al. (US Patent Application Publication No. 2003/0231437) in view of Tuttle et al. (US Patent Application Publication No. 2003/01322494).

Regarding claim **29**, Childress et al. disclose a memory wafer ([0018]) comprising:

a first surface of 9, 109 (figs. 1 & 2) having memory chips disposed thereon, the memory chip defining an exterior face 150 (fig. 2) of the memory wafer (note: the MTJ is use in nonvolatile memory elements or cells for MRAM ([0002]); substrate 9 (fig. 1) would be a silicon (memory) wafer if the device is a memory cell ([0018]). Therefore, it is fair to say that the silicon wafer 9 having memory chips for MRAM).

a second surface of 9, 109 (figs. 1 & 2) opposite the exterior face; and

a top magnetically permeable shield layer (made of permalloy (NiFe) as the claimed permeable shield layer) on top of surface 150 (not shown) ([0021]).

Childress et al. do not explicitly show means for protecting the memory cells from stray magnetic fields.

However, Tuttle et al. show the undesirable external magnetic field can also call stray fields ([0019]). The magnetically permeable foils 26 and 28 (fig. 1) are attached to top and bottom outer surfaces of the chip used as shields from stray fields ([0028]). The magnetically permeable layers of Childress device are identical to Tuttle shields. Therefore they can be used as means for protecting from external field or stray fields.

Regarding claim **30**, Childress et al. disclose the magnetically permeable layer is a permalloy (NiFe) and is a soft magnetic material.

11. Claims **31** and **32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Childress et al. (US Patent Application Publication No. 2003/0231437) in view of Tuttle et al. (US Patent Application Publication No. 2003/01322494) and further in view of Rizzo et al. (US Patent Application Publication No. 2004/0000415).

Art Unit: 2818

12. Regarding claim **31**, Childress et al. and Tuttle et al. disclose the claimed invention of claims 29 and 30 except for the magnetically permeable shield layer has permeability of greater than 100.

Rizzo et al. show a shielding material can have a permeability 1,000 – 10,000 depending on the particle size ([0051] and [0053]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the magnetically permeable shield layer of Childress and Tuttle with a layer having a permeability of greater than 100 as taught by in order to get superparamagnetic behavior for very effective magnetic field shielding.

Regarding claim **32**, Rizzo et al. disclose the magnetically permeable shield layer has a coercivity of less than 10 Oersteds ([0043]).

### ***Response to Argument***

13. Applicants' arguments have been fully considered but they are not persuasive.

14. The applicants argue:

Childress et al. fails to disclose a memory wafer having memory chips disposed thereon."

The examiner responds:

As set forth in claims 1 – 17 and 18 – 32, the MTJ is use in nonvolatile memory elements or cells for MRAM ([0002]); substrate 9 (fig. 1) would be a silicon (memory) wafer if the device is a memory cell ([0018]). Therefore, it is fair to say that the silicon wafer 9 having memory chips (MTJ) for MRAM).

For the above reasons, it is believed that the rejections should be sustained. Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

Art Unit: 2818

**Conclusion**

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran *LT*

April 21, 2005

  
David Nelms  
Supervisory Patent Examiner  
Technology Center 2800